providing an adjustment input to produce a positive 2π adjustment signal if a tested signal is greater than a first reference value and produce a minus 2π adjustment signal if the tested signal is less than a second reference value.

REMARKS

Claims 1, 2, 3, 6, 8, 9, and 11 have been cancelled.

Claims 5 and 12 have been amended in this response.

Claims 32 to 35 are new.

Thus, claims 4, 5, 7, 10, 12–31, 32 to 35 are pending in this application.

It is respectfully submitted that claims 32 to 35 are directed to the same invention as the elected claims, that a new search is not necessary and examination and allowance is requested.

Regarding Claims 4, 5, 7, 10, and 31

The indication that Claims 4, 5, 7, 10, and 31 are allowed has been noted with appreciation.

It is noted however that even though claim 5 is allowed, alleged grounds for the rejection of claim 5 are recited in the office action. Claim 5 has therefore been amended a second time in response to the alleged grounds of rejection.

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Regarding Claims 5 (Twice Amended) and 12 (Amended).

Claims 5 and 12 stand rejected under 35 USC 112, first paragraph as indefinite for reciting the allegedly unsupported terms "coefficient multiplier" and "coefficient multiplier circuitry". Claims 5 and 12 have been amended to exclude the allegedly unsupported terms, reconsideration and allowance of claim 5 (Twice amended) and claim 12 (Amended) is requested.

Regarding Claims 13, 14, to 19, 25, 27, and 28

Claims 13, 14, to 19, 25, 27, and 28 stand rejected under 35 USC 102(b) as being anticipated by U.S. Patent 4,766,495 of Kobayashi et al. .

Claims 14, 15, 16, and 17 each depend on Claim 13 (Twice amended).

The rejections of Claims 13 (Twice amended), 14, 15, 16, and 17 are respectfully traversed.

In regards to Claim 13 (Twice amended) it is submitted that Kobayashi does not disclose nor teach all the limitations of claim 13. The office action states "Kobayashi discloses the claimed providing a circuit, inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit (fig 5 items 21 and 22), inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset that is added to the output (fig 5 adjustments coefficients K2 and K1 will change the level of output Dvec), adding the adjustment signal to the input signal

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(figure 5, the signal K2 x DoN+1) is added to the delayed or filtered signal K1 x DoN)". This statement is respectfully traversed.

In Kobayashi fig. 5 the examiner points to Delay Circuit 22 as providing the filter function and therefore correspondingly signal Do(N+1) is the input signal disclosed. Thus, Kobayashi does not disclose nor teach the limitation "adding the adjustment signal to the input signal" since in Kobayashi fig. 5 no adjustment is added to the signal Do(N+1). Kobayashi fig. 5 does disclose multiplying an adjustment signal (K2) by the input signal (Do(N+1)), but multiplying signals together and adding signals to one another are known to be distinct in the art. Kobayashi fig. 5 also discloses that the product of the input signal (Do(N+1)) and the adjustment signal (K2) is added by adder 25 (in Kobayashi fig. 5). However, this adding of the product does **not** produce an equivalent effect to adding the input signal (Do(N+1)) and the adjustment signal (K2) together. Scaling a signal by multiplying and offsetting a signal by adding are crucially different – scaling a zero signal will have no effect on it, but offsetting a zero signal makes it non-zero. Therefore, it is respectfully submitted that claim 13 (Twice amended) should be allowed under 35 USC 102(b). Allowance of claim 13 is requested.

Furthermore, it is respectfully submitted that since claims 14, 15, 16, 17 each depend from claim 13 (Twice amended) they should be allowed under 35 USC 102(b) for at least the same reasons as claim 13 (Twice amended). Allowance of claims 14, 15, 16, and 17 is requested.

Claims 19, 25 and 27 each depend on Claim 18 .

The rejections of Claims 18(Amended), 19, 25, 27 and 28 (Twice amended) are respectfully traversed.

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In regards to Claims 18(Amended) and 28 (Twice amended), the office action states "Kobayashi inherently discloses constraining a phase signal within a finite preset range (in order to correct the phase, the output phase must be inherently constrained within a preset range)." This statement is respectfully traversed. . It is respectfully submitted that the Examiner has not made the required showing of rationale or evidence tending to show inherency. See MPEP Section 2112, fourth paragraph entitled "EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY". Moreover, Kobayashi simply does not disclose or teach the **constraining** of phase angles as the term is understood in the relevant arts or in non-specialized language usage. For example, Figure 7 of the drawings in the present application, a suitable example preset range of 4π (720 degrees from $-\pi$ to $+3\ \pi$) is shown. It is respectfully submitted, therefore, that Kobayashi does not teach, disclose or suggest all the limitations of Claims 18 (Amended) or 28 (Twice amended), and that these claims are allowable under 35 USC 102(b). Moreover, Claims 19, 25 and 27 each depend upon Claim 18(Amended) and are therefore allowable for at least the same reasons as Claim 18(Amended). Allowance of Claims 18 (Amended), 19, 25, 27 and 28 (Twice amended) is requested.

Regarding claims 20, 21, 22, 23, 24, 26, 29, and 30

Claims 20, 21, 22, 23, 24, 26, 29, and 30 stand rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 4,766,495 of Kobayashi et al. ("Kobayashi") in view of the Video Demystified handbook by (Keith Jack). ("Jack").

The office action states *"Kobayashi fails to disclose wherein the correction signal is a multiple of 2pi. Kobayashi discloses adjusting and converting the phase of a signal. The*

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Video Demystified handbook teaches by adjusting the hue from 0 deg to 360 deg can compensate for transmission problems."

The office action further states *"Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kobayashi to include the claimed correction signal having an integer multiple of 2pi to compensate for transmission problems"*. This statement is respectfully traversed. Jack teaches away from the combination in two ways. Firstly, Jack teaches **to change hue** by introducing a phase offset (see Jack, section entitled "**Hue Adjustment**"). Conversely the present application teaches to adjust phase by an integer multiple of 360 deg to **avoid any change in hue**. Secondly Jack teaches to change phase to compensate for **transmission problems**. Conversely the present application teaches teaches to adjust phase by an integer multiple of 360 deg to mitigate problems **other than transmission problems**, specifically to mitigate problems caused by, inter alia, continually advancing phase angles. Thus it is improper to combine the circuit of Kobayashi with the 360 deg phase angle adjustment of Jack and rejection of claim 20 under 35 USC 103(a) is improper. See MPEP 2145-X-D-2 "References cannot be combined where the references teaches away from the combination."

For the foregoing reasons, it is respectfully submitted that all pending claims are now in condition for allowance. Should the Examiner wish to discuss any aspect of this case via telephone, please contact attorney Gerald Parsons (registrant 24486) at (415) 217-6000.

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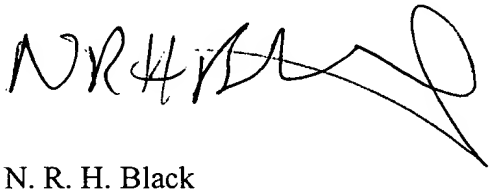
Respectfully submitted,



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Claim 5 has been amended:

5. (Twice Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered,

wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input,

and wherein the coefficient circuit includes an input summer and a gain amplifier having a gain.

Claims 32 to 35 are new:

32. (New) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

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a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input,

wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a first reference value and produce a positive 2π adjustment signal if the tested signal is less than a second reference value.

33. (New) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input,

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wherein the adjustment control logic is adapted to produce a positive 2π adjustment signal if a tested signal is greater than a first reference value and produce a minus 2π adjustment signal if the tested signal is less than a second reference value.

34. (New) A method comprising:

providing a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

providing a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

providing an adjustment input to produce a minus 2π adjustment signal if a tested signal is greater than a first reference value and produce a positive 2π adjustment signal if the tested signal is less than a second reference value.

35. (New) A method comprising:

providing a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

providing a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the

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at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

providing an adjustment input to produce a positive 2π adjustment signal if a tested signal is greater than a first reference value and produce a minus 2π adjustment signal if the tested signal is less than a second reference value.

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Version with markings to show changes made

5. (Twice Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered,

wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input,

and wherein the ~~output of the at least one coefficient circuits is to a delay and the output of delay sent to the at least one coefficient circuits~~ **coefficient circuit includes an input summer and a gain amplifier having a gain**.

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